IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Om P. Agrawal; Howard Tang; Jack Wong		
Assignee:	Lattice Semiconductor Corporation		
Title:	Upgradeable And Reconfigurable Programmable Logic Device		
Serial No.:	Unknown	Filing Date:	Herewith
Examiner:	Unassigned	Group Art Unit:	Unknown
Docket No.:	M-15311 US		

Irvine, California
February 20, 2004

COMMISSIONER FOR PATENTS
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

UNDER 37 C.F.R. §1.97 AND § 1.98

Dear Sir:

Pursuant to 37 C.F.R. §1.97 and §1.98, Applicant calls the following documents (copies enclosed) to the attention of the Examiner. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom. Note that U.S. patent application no. 10/439,602 is being submitted for the Examiner to consider regarding double patenting.

A PTO form 1449 listing these documents is enclosed.

Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

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2. a representation that a search has been made, or

3. an admission that the information cited herein is, or is considered to be material to patentability as defined in §1.56(b).

Applicant(s) believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 50-2257. Please deduct any additional fees from, or credit any overpayment to the above-noted Deposit Account.

Express Mail #EV411212055US

Respectfully submitted,

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U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15311 US	Unassigned
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant(s)	
(Use several sheets if necessary)	Om P. Agrawal; Howard Tang; Jack Wong	
	Filing Date	Group
	Herewith	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,548,228	08/20/1996	Madurawe			
	AB	5,696,455	12/09/1997	Madurawe			
	AC						
	AD						
	AE						
	AF						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AG							
	AH							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AI	Actel Corporation, "ProASIC PLUS Flash Family FPGAs", v3.4 December 2003, pages i through iv and 1-1 through 1-64 & 2-1 through 2-67 & 2-1 through 2-7 (list of changes).
	AJ	Lattice Semiconductor Corporation, "ispXPGA™ Family", Preliminary Data Sheet, September 2003, pages 1-112.
	AK	U.S. Patent Application Serial No. 10/439,602, filed on 05/16/2003, entitled "Non-Volatile And Reconfigurable Programmable Logic Devices"

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.